AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior listing of claims for the present application.

Claims 1-5 (Canceled).

6. (Currently amended) A method for forming a memory device, comprising:

forming a gate dielectric on a semiconductor substrate;

forming source and drain regions on opposite sides of said gate dielectric;

forming a floating gate on said gate dielectric;

forming ~~a silicon-doped~~ an Al_2O_3 layer by chemical vapor deposition on said floating gate; ~~and~~

subsequently implanting silicon into said CVD deposited Al_2O_3 layer by ion implantation to form a silicon-doped Al_2O_3 layer; and

forming a control gate on said silicon-doped Al_2O_3 layer.

7. (Original) The method of claim 6, wherein said step of forming said silicon-doped Al_2O_3 layer is performed at an energy of approximately 10keV and at a dose of approximately $1x10^{14}$ /cm^2 to $1x10^{15}$/cm^2.

8. (Original) The method of claim 6 further comprising forming a silicide layer on top of said control gate.

9. (Original) The method of claim 6, wherein said gate dielectric is formed of a material selected from the group consisting of oxynitride and oxide.

10. (Original) The method of claim 6, wherein said memory device is a flash memory device.

Claims 11-26 (Canceled).

27. (New) A method of forming a semiconductor device, said method comprising:

forming a first conductive layer over a semiconductor substrate;

forming an Al_2O_3 layer over said first conductive layer;

subsequently implanting dopants into said Al_2O_3 layer by ion implantation to form a dopant-implanted Al_2O_3 layer, wherein said dopant-implanted Al_2O_3 layer has a non-uniform doping profile; and

forming a second conductive layer over said dopant-implanted Al_2O_3 layer.

28. (New) The method of claim 27, further comprising forming a silicide layer on top of said conductive layer.

29. (New) The method of claim 27, wherein said semiconductor device is a capacitor.

30. (New) The method of claim 27, wherein said semiconductor device is part of a transistor gate stack which stores charge.

31. (New) The method of claim 30, wherein said transistor gate stack is part of a flash memory cell.

32. (New) The method of claim 27, wherein said semiconductor device is DRAM.

33. (New) The method of claim 27, wherein said step of ion implantation of dopants into the Al_2O_3 layer is conducted with energy of approximately 10keV.

34. (New) The method of claim 27, wherein said step of ion implantation of dopants into the Al_2O_3 layer is conducted with silicon at a dose of approximately $1x10^{14}$ /cm^2 to $1x10^{15}$/cm^2.

35. (New) The method of claim 27, wherein said first conductive layer is formed in a reaction chamber at a temperature from about 550 to about 650°C.

36. (New) The method of claim 35, wherein said reaction chamber is held at a pressure of less than approximately 2 Torrs.

37. (New) The method of claim 27, wherein said first conductive layer is implanted with dopant ions to lower the resistivity of said first conductive layer.

38. (New) The method of claim 27, wherein said Al_2O_3 layer is CVD deposited with uniform coverage of approximately 0.2 to 1.0μ.

39. (New) The method of claim 27, wherein said dopant-implanted Al_2O_3 layer is annealed at a temperature from about 600 to about 950°C.

40. (New) The method of claim 27, wherein said second conductive layer is formed in a reaction chamber at a temperature from about 550 to about 650°C.

41. (New) The method of claim 40, wherein said reaction chamber is held at a pressure of less than approximately 2 Torrs.

42. (New) The method of claim 27, wherein said second conductive layer is implanted with dopant ions to increase the conductivity of said second conductive layer.

43. (New) The method of claim 27, further comprising forming a refractory metal over said second conductive layer.

44. (New) A method of forming a memory device comprising:

forming a gate dielectric on a semiconductor substrate between source and drain regions;

forming a floating gate over said gate dielectric;

forming a dopant-implanted insulating layer over said floating gate, said dopant-implanted insulating layer being formed by CVD deposition and ion implantation, wherein said dopant-implanted insulating layer has a dopant gradient; and

forming a control gate over said dopant-implanted insulating layer.